A Switched DC Link Inverter for Five-Level Output with Single Input Source

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***Abstract*—This paper discusses a new hybrid topology for multilevel inverters utilizing a switched capacitor DC link. Input source is connected to the DC link capacitors through four power electronic switches. The switched capacitors based DC link is combined with an H-bridge part along with an auxiliary switch, thereby generating a five-level output. The operating voltage approximately twice the input voltage, and hence a boost operation can be implemented. An appropriate control scheme is presented and simulation results are discussed along with experimental validations. A comparison with the conventional topologies shows that the proposed topology requires lesser number of components.**

Keywords-Multilevel inverters, switched capacitor topologies, modulation schemes

I. INTRODUCTION

IN past few decades, multilevel voltage source inverters have been established as cost-effective and efficient solution for high power/high and medium voltage DC to AC conversion applications [1]. A multilevel inverter (MLI) utilises multiple input DC levels (obtained from DC sources and/or capacitors) and power semiconductor devices to synthesize a stepped waveform, imitating the desired sinusoidal waveform. The overall operating voltage level is much greater than the voltage blocked by the power switches [2]. The multilevel waveform has a better harmonic profile as compared to that of a two level waveform obtained from conventional inverters. Higher efficiency, reduced d*v*/d*t* stresses on the load and possibility of fault tolerant operation are some of the other attractive advantages of MLIs [3]. MLIs have also been used for low power applications apart from their applications in medium/high power and high voltage systems [4,5].

Among various topologies for MLIs, the most popular topologies are: diode clamped converter, flying-capacitor converter and cascaded H-bridge converter [6, 7]. Diode clamped and flying capacitor converter topologies are generally implemented with a single DC source, but the device count increases rapidly with the number of output levels, thus leading to complex control and higher costs. Also, voltage balancing of DC link capacitors needs to be taken care of [7,8]. Cascaded H-bridge (CHB) converter topology can be implemented for higher number of levels in the output by series connection of H-bridge cells, each having its own electrically isolated DC source. CHB topology excels over diode clamped and flying capacitor converter topology in terms of modularity and active device count, thus it was the one to get commercialized at early stages. Still, it becomes mandatory to use a transformer with multiple secondary windings when only a single source is available, thereby making the system more expansive, complicated and bulky [6-8].

In past few years, newer topologies have been proposed to overcome aforesaid challenges. Structures such as the switched capacitor (SC) inverter require only one DC source to synthesize higher number of output voltage levels, along with the capability of increasing the output voltage as compared to the input value [9-15]. This boosting feature reduces the transformation ratio of the input transformer or can eliminate it, thereby reducing the overall costs.

In this paper, a novel multilevel topology based on a switched DC link is presented. The switched DC link circuit is used to balance the capacitor voltages under various load conditions, and they also participate in synthesizing the output voltage levels. H-bridge part along with the auxiliary switch helps feed the AC load with a five-level voltage waveform. This topology also increases the amplitude of the output voltage to twice the input voltage value. Besides, it can be extended to any number of levels in the output. The operation of the proposed structure has been discussed in this paper and proposed concepts are verified with the help of simulations for a five-level single-phase inverter and low-voltage low-power experimental prototype.

Section II introduces the proposed topology and explains its working with various operating states. Section III presents an appropriate switching procedure for the topology. Section V shows the simulated and experimental results of the proposed inverter whereas in section IV, the proposed topology is compared with the conventional topologies. Finally, conclusions are presented in section VI.

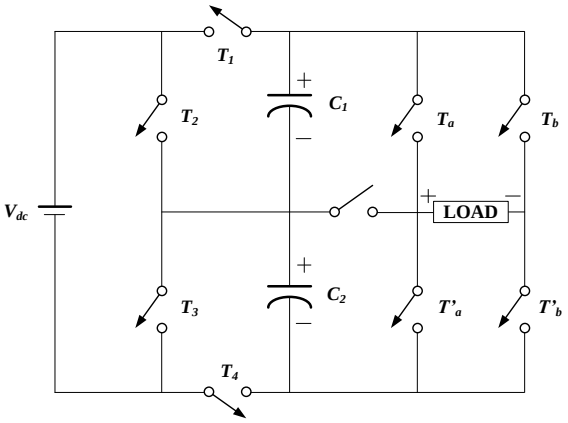


Figure 1. The structure of the proposed five level inverter

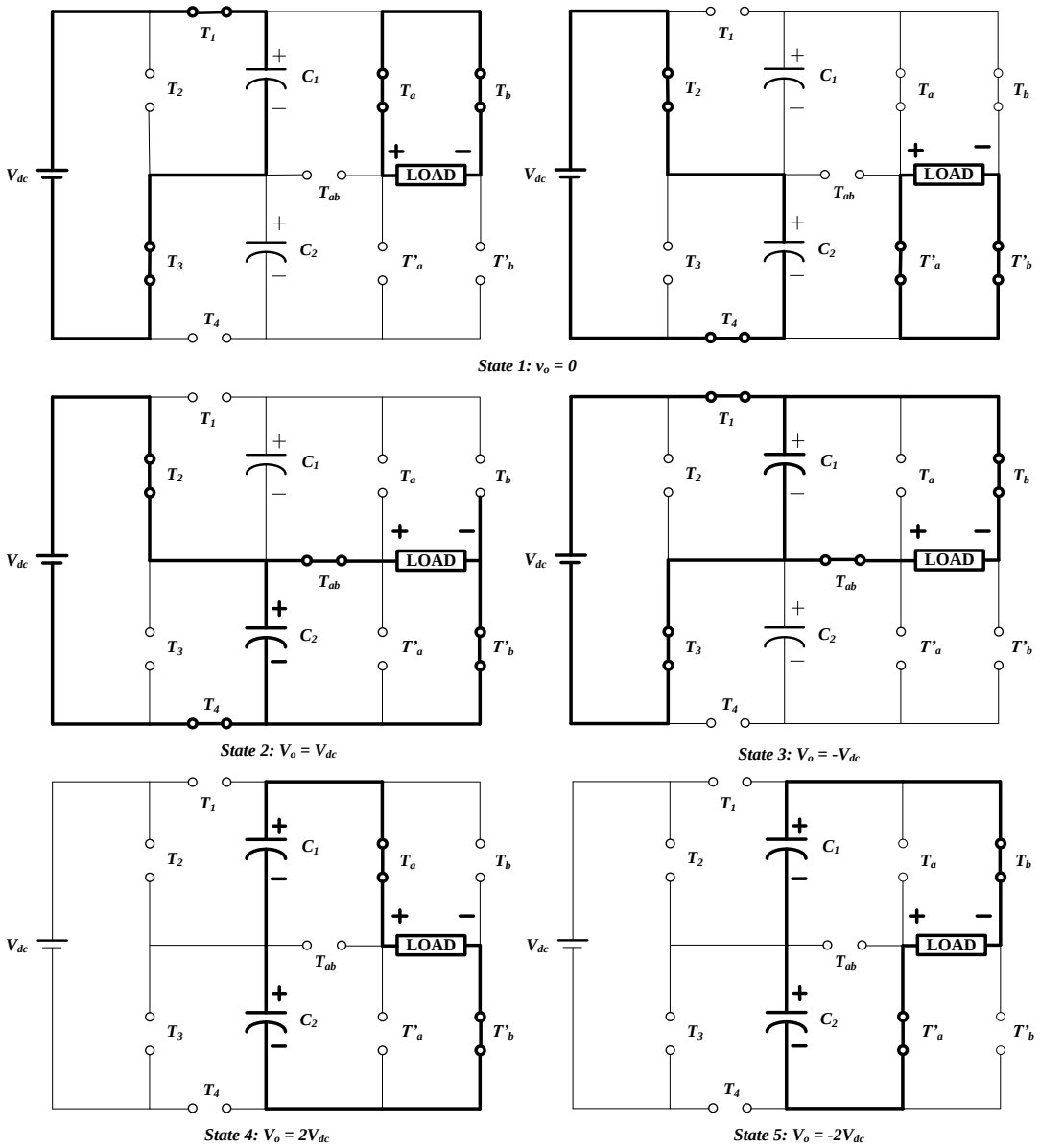


Figure 2. Various operating states of the proposed five level inverter

II. PROPOSED TOPOLOGY: STRUCTURE AND OPERATION

The proposed topology for a five-level inverter is shown in Fig.1.It is basically a combination of a switched capacitor (SC) circuit and an H-bridge cell. SC part consists of four switches T_1,T_2,T_3 and T_4whereasT_a,T_b,T_a'and T_b' are the switches of H-bridge cell. All these switches are called main switches. T_{ab} is the auxiliary bidirectional switch which is responsible for connecting both parts [16]. C_1 and $C_2$are the DC-link capacitors andV_{dc} is the input voltage source.

T_1, T_3 and T_2,T_4 are complimentary pair switches i.e. when one is operated other is off. C_1gets charged when T_1, T_3 are switched ON and$C_2$is charged when T_2, T_4 are ON. Both capacitors are charged by connecting them across the source. T_a,T_b,T_a'and T_b'take part in polarity generation at the output.

Operation of the five-level inverter is described in five states which are shown in Fig. 2. Table I enlists the switches which are in ON state during various states of operation. Output voltage corresponding to each state is also shown. The state of the DC- link capacitors are explained by giving some notations for easy understanding in below table. Here'0','1'and '-1'indicate uncharged, charging and discharging modes of capacitor respectively while '#' denotes that the capacitor is in the charged state. H-bridge switches are stressed more because they have to be operated in all the states accordingly.

TABLE I. OPERATING STATES

Parameters → Operating States ↓	ON State Switches	Capacitor Status	Output Voltage
State 1	T_1, T_3, T_a, T_b or T_2, T_4, T_a', T_b'	$C_1=1, C_2=0$ or $C_1=0, C_2=1$	0
State 2	T_2, T_4, T_{ab}, T_b'	$C_1=\#, C_2=1$	V_{dc}
State 3	T_1, T_3, T_{ab}, T_b	$C_1=1, C_2=\#$	$-V_{dc}$
State 4	T_a, T_b'	$C_1=C_2=-1$	$2V_{dc}$
State 5	T_a', T_b	$C_1=C_2=-1$	$-2V_{dc}$

All the operating states are explained as follows:

State 1: In this state, zero voltage level is produced at the output. As observed from table I, this state possesses redundancy. Thus either capacitor, C_1 or C_2 could be in charging state.

State 2: Switches T_2 and T_4 are activated here. C_1 remains in the charged state while C_2 gets connected across the source to be in the charging state. At the same time, T_{ab} and T_b' are turned ON so that V_{dc} appears across the output.

State 3: Similar to state2, output voltage $-V_{dc}$ is produced by activating switches T_1, T_a, T_{ab} and T_b. C_1 is in charging state while C_2 remains in charged state.

State 4: H-bridge switches T_a and T_b' are turned ON which provides a discharging path to both the capacitors to generate $2V_{dc}$ at the output.

State 5: Similar to state 4 in operation. Only difference is that switches T_b and T_a' are activated instead of T_a and T_b'.

Combining these five states gives one cycle of operation and this procedure is repeated for further cycles.

III. SWITCHING METHODOLOGY

There are different types of switching schemes are available based on switching frequency required which can be employed for the operation and control of multilevel inverters. These are broadly classified as high switching frequency and fundamental switching frequency modulation strategies [17,18]. Performance of the proposed five-level inverter is examined by using universal control scheme. This control scheme can be used to implement any sinusoidal PWM strategy for multilevel inverter [19].

The whole scheme can be implemented for any number of levels in the output as shown in Fig. 3. The carrier signals which are above and below zero axis are designated as C_x and C_y. Wherever the reference is higher than carrier signal (C_x) comparator produces'1', otherwise '0' .In similar manner if reference signal is greater than carrier (C_y) then comparator produces'0' at its output, otherwise '-1'. Triangular waveforms of suitable frequency are considered carrier signals and reference waveform is taken as sinusoidal waveform in this scheme. Comparator outputs are then summed up to give the aggregated signal which consists of same levels as required in output. Individual signals are extracted from the aggregated signal by equating it to values corresponding to each level. The look up table given in table II is then utilized to determine that a particular switch is active for which levels of aggregated signal. Individual signals corresponding to those levels are ORed together and then fed to that switch.

TABLE II.LOOK-UP TABLE

Level of Aggregated Signal	Level of output voltage	Switch States (1 = ON, 0 = OFF)								
		T_1	T_2	T_3	T_4	T_a	T_b	T_a'	T_b'	T_{ab}
2	$2V_{dc}$	0	0	0	0	1	0	0	1	0
1	V_{dc}	0	1	0	1	0	0	0	1	1
0	0	1	0	1	0	1	1	0	0	0
		0	1	0	1	0	0	1	1	0
-1	$-V_{dc}$	1	0	1	0	0	1	0	0	1
-2	$-2V_{dc}$	0	0	0	0	0	1	1	0	0

Waveforms for generation of switching pulses for proposed five-level inverter are presented in Fig.4. The modulation index M which is generalized for multilevel inverters is given by,

$$M = \frac{2A_{ref}}{(N-1)A_c}$$

where A_{ref} and A_c are the amplitudes of the reference and carrier signal respectively and N is the number of levels in the output voltage.

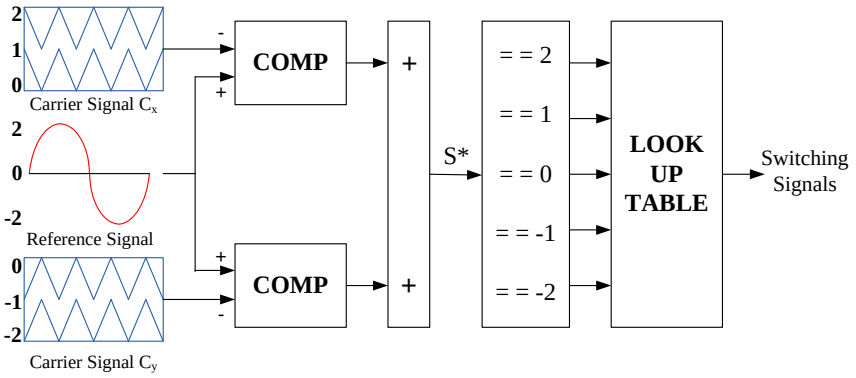


Figure 3. Generalized block diagram of the overall modulation scheme.

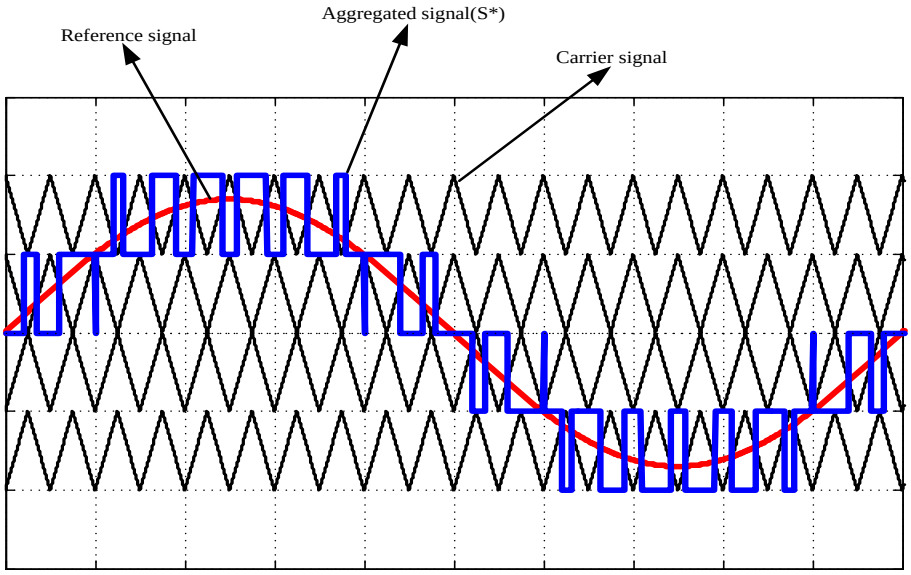


Figure 4. Waveforms for generation of aggregated signal for switchning pulses of the switches .

IV. Comparison with Conventional 5-Level Topologies

A relative comparison has been made between the five level inverter and conventional five level topologies on account of total number of components required. This is shown in table IV. The proposed five level inverter does not require clamping diodes or floating capacitors. DC link capacitors are reduced as compared to neutral point clamped and flying capacitor five level inverter. Proposed inverter utilizes a single source whereas two isolated sources are required for the CHB inverter to synthesize similar output voltage waveform. The attractive feature of the proposed inverter is that it has inherent boosting capability which is absent in all the three conventional five level inverters. This feature helps in reducing the transformation ratio of the transformer or even eliminates it thereby reducing the size, weight and total cost of inverter.

TABLE III
Comparison of Proposed Topology with Conventional 5-Level Topologies

Topology	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed Topology
Clamping Diodes	*12*	*0*	*0*	*0*
Floating Capacitors	*0*	*6*	*0*	*0*
DC-link Capacitors	*4*	*4*	*0*	*2*
Switches (Main)	*8*	*8*	*8*	*8*
Switches (Auxiliary)	*0*	*0*	*0*	*1*
Input DC source	*1*	*1*	*2*	*1*
Total Components	*25*	*19*	*10*	*12*
Boosting	*NO*	*NO*	*NO*	*YES*

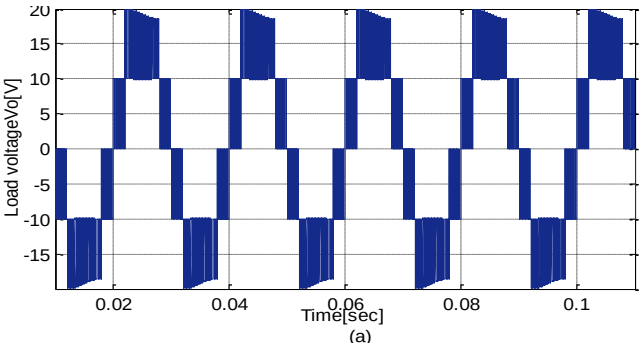
capability				

V. SIMULATION RESULTS

The proposed five-level inverter is simulated using SimPowerSystem toolbox in MATLAB/SIMULINK environment. The parameters used in simulation as well as in experimental are listed in the table III. Fig. 5 shows the simulated output voltage, output current and capacitor voltages waveforms of the proposed inverter whereas Fig. 6 shows the experimental results for same. Output voltage is stepped up to double the input voltage. This is observed from both the simulation as well as experimental results. Experimental results are showing close proximity with the simulation results. The distortion in the experimental results is due to the presence of ripples in capacitor voltage. In order to reduce these ripples to minimum value, large capacitors are required.

TABLE IV. SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters		**Value**
MainSwitches	*Resistance (R_{INT})*	*0.001Ω*
	Snubber resistance(R_{SUB})	*100 kΩ*
Auxiliary Switch	*Resistance (R_{INT})*	*0.001Ω*
	Snubber resistance(R_{SUB})	*100 kΩ*
Input Voltage	V_{dc}	*100*
Switching Frequencies	$f_{carrier}$	*1000 Hz*
	f_{ref}	*50 Hz*
DC link capacitors	C_{DC}	*1000μF*
	R_C	*1 mΩ*
LOAD	*Resistance(R_L)*	*30 Ω*
	Inductance(L)	*3.25 mH*



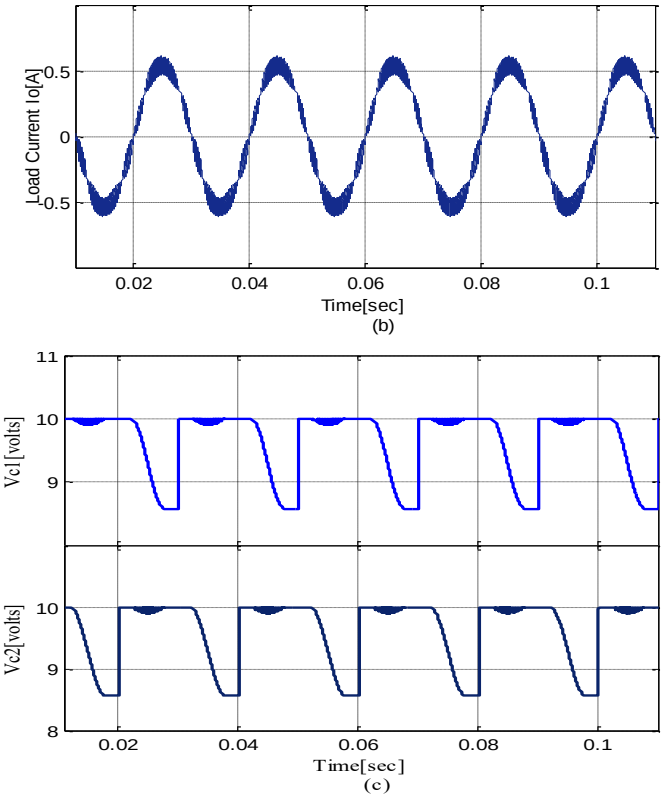


Figure 5. Simulated waveforms of proposed five level inverter for a) Load voltage, b) Load current and c) Voltage across both capacitors C_1 and C_2

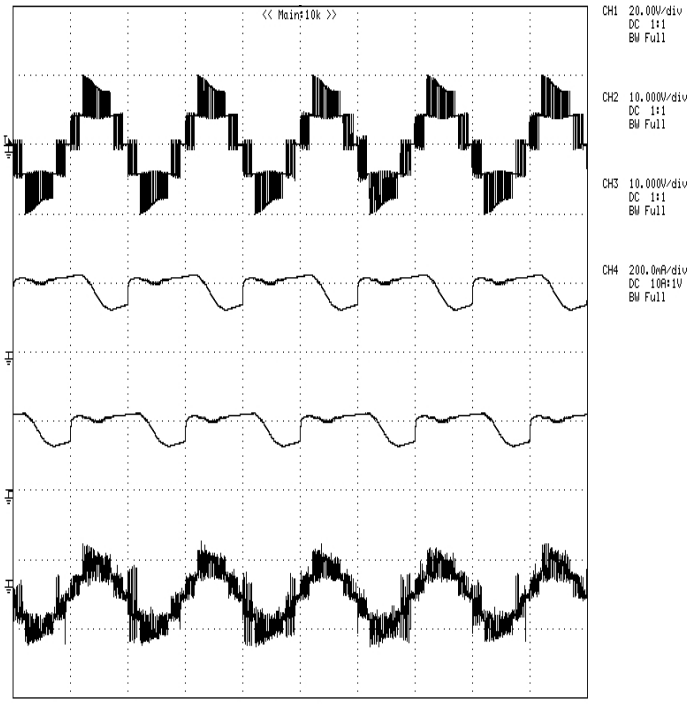


Figure 6. Experimental results for load voltage, capacitor (C_1,C_2)voltages and load current of proposed five level inverter respectively.

VI. CONCLUSIONS

In this paper a new topology for multilevel inverters is proposed. Input DC source is connected to the switched capacitor part. This part plays the role of stepping up the voltage as well as generating levels at the output. H-bridge plays the role of polarity generation at the output. Here output voltage is increased to approximately double the input voltage. This is useful in reducing the transformation ratio of transformer thereby reducing the size and overall cost of inverter. It can be concluded that by balancing both capacitors voltages, boosting of output voltage is possible. Reduction of ripples in capacitor voltage can be achieved by choosing proper values of capacitance.

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